

		R C Patel Institute of Technology, Shirpur					
		Department of Electronics & Telecommunication					
Class: SY B.TECH E & TC (A)		Year: 2025-26			Sem II	Class Room No. 92	
W E F (02/03 /2026)							
SR.No	Time	Monday	Tuesday	Wednesday	Thursday	Friday	Saturday
	10.10 To 11.00		IC_PJD	IC_PJD	MCA_SGP		
1	11.00 TO 11.50	MCA_SGP	DSA_VRP	UHV_MLP	SS_ABJ_TUTO_A2	MCA_SGP	Intro VLSI_NLL
2	11.50 TO 12.40	SS_ABJ	UHV_MLP	MCA_SGP	IC_KHS	DSA_VRP	UHV_MLP
	12.40 TO 1.45	Long Recess					
3	1.45 TO 2.35	DSA_VRP	IC_KHS	DMM_MLP/THJ	DMM_MLP/THJ	Intro VLSI_NLL	Intro VLSI LAB_B2_NLL EL 6
4	2.35 TO 3.25	Intro VLSI_NLL	DSA_VRP	DMM_MLP/THJ	DMM_MLP/THJ	Intro VLSI_NLL	
	3.25 TO 3.40	Short Recess					
5	3.40 TO 4.30	IC_A1_EL 4 MCA_A2_EL 6 DSA_A3_EL 5	DSA_A2_EL 5 MCA_A3_EL 6 DTL_A1_EL 3	IC_A3_EL 4 DSA_A1_EL 5* DTL_A2_EL 3	DTL_A3_EL 3 MCA_A1_EL 6 IC_A2_EL 4	Intro VLSI LAB_B1_NLL EL 6	SS_ABJ
6	4.30 TO 5.20						SS_ABJ_TUTO_A1
Library Hours							
SR	THEORY		PRACTICAL		TUTORIAL		
1	Integrated Circuit (IC)	Dr P J deore Dr K H Sonawane	Integrated Circuit (IC)	Dr K H Sonawane	Signals & Systems (SS)	Dr A B Jayswal	Note: 80 % attendance is compulsory. Candidate failing to complete this will be detained
2	Microcontroller & Applications (MCA)	Dr R D Badgular Prof S G Patil	Microcontroller & Applications (MCA)	Prof S G Patil			
3	Data Structures & Algorithms (DSA)	Dr V R Patil	Data Structures & Algorithms (DSA)	Dr M B dembrani Dr V R Patil*			
4	Signals & Systems (SS)	Dr A B Jayswal	Design Thinking Lab (DTL)	Dr V S Patil/ Dr A B Jayswal			
5	Universal Human Values (UHV)	Prof M L Patel					
6	Digital Markting	Prof M L Patel / Dr T H Jaware					
7	Intro VLSI	Dr N L Lokhande	Intro VLSI	Dr N L Lokhande			
8							
Time Table Incharge					 HOD, E&TC R. C. Patel Institute of Technology Shirpur, Dist: Dhule (MS)		
 Prof P M GOAD							