



R C Patel Institute of Technology, Shirpur
Department of Electronics & Telecommunication



Class: SY B.TECH E & TC (B)

Year: 2025-26

Sem II

Class Room No. 91

W E F (02/03 /2026)

SR.No	Time	Monday	Tuesday	Wednesday	Thursday	Friday	Saturday
	10.10 To 11.00				DSA_VRP	DSA_VRP	MCA_SGP
1	11.00 TO 11.50	DSA_B1_Research Lab* DTL_B2_EL 3* IC_B3_EL 4*	IC_PJD	IC_PJD	DSA_VRP	SS_ABJ_TUTO_B2	Intro VLSI_NLL
2	11.50 TO 12.40		MCA_RDB	IC_KHS	UHV_MLP	SS_ABJ	DSA_VRP
	12.40 TO 1.45	Long Recess					
3	1.45 TO 2.35	UHV_MLP	MCA_RDB	DMM_MLP/THJ	DMM_MLP/THJ	Intro VLSI_NLL	Intro VLSI LAB_B2_NLL EL 6
4	2.35 TO 3.25	Intro VLSI_NLL	IC_KHS	DMM_MLP/THJ	DMM_MLP/THJ	Intro VLSI_NLL	
	3.25 TO 3.40	Short Recess					
5	3.40 TO 4.30	SS_ABJ	DTL_B1_EL 2 IC_B2_EL 4 MCA_B3_Research Lab	MCA_SGP	DTL_B3_EL 2 MCA_B1_EL 5 DSA_B2_Research Lab	Intro VLSI LAB_NLL EL 6	IC_B1_EL 4 DSA_B3_Research Lab MCA_B2_EL 2
6	4.30 TO 5.20	SS_ABJ_TUTO_B1		UHV_MLP			
	0	Library Hours					

SR	THEORY	PRACTICAL	TUTORIAL
1	Integrated Circuit (IC) Dr P J deore Dr K H Sonawane	Integrated Circuit (IC) Dr K H Sonawane Dr P M Goad*	Signals & Systems (SS) Dr A B Jayswal
2	Microcontroller & Applications (MCA) Dr R D Badgular Prof S G Patil	Microcontroller & Applications (MCA) Dr R D Badgular	
3	Data Structures & Algorithms (DSA) Dr V R Patil	Data Structures & Algorithms (DSA) Dr V R Patil Dr T H Jaware*	
4	Signals & Systems (SS) Dr A B Jayswal	Design Thinking Lab (DTL) Dr T H Jaware Dr B V Patil*	
5	Universal Human Values (UHV) Prof M L Patel		
6	Digital Marketing Prof M L Patel		
7	Intro VLSI Dr N L Lokhande	Intro VLSI Dr N L Lokhande	

Note: 80 % attendance is compulsory. Candidate failing to complete this will be detained

8	Time Table Incharge Prof P M GOAD		HOD HOD, E&TC R. C. Patel Institute of Technology Shirpur, Dist. Dhule (15%) Prof Dr V S Patil
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